UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/516,082	03/01/2000	Satoshi Murakami	SEL163	3545

7590 12/03/2003

Cook Alex Mcfarron Manzo
Cummings & Mehler LTD
200 West Adams ST
Suite 2850
Chicago, IL 60606

EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/516,082	MURAKAMI ET AL.	
	Examin r	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46-88* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *46-88* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *21* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 59, 65, 68 and 86 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 59 recites the limitation "wherein the pixel matrix circuit and the driver circuit" in the last line of said claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 68 recites the limitation "the first electrode" in lines 5-6 of said claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the

reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 46, 47, 56, and 62 are rejected under 35 U.S.C. 102(e) as being anticipated by Kadota et al. 5,818,550. Kadota discloses (see, for example, FIG. 1) a semiconductor device comprising a first thin film transistor formed over a TFT substrate (insulating surface) 0 wherein the first thin film transistor comprises a semiconductor film 2, source and drain region S/D, channel forming region, gate insulating film, gate electrode 3; first inter-layer insulating film (interlayer insulating film) 4, electrodes (conductive layer) 7, color filter 9R/9G/9B, and pixel electrode 1. The color filter has a flattened surface.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 48 thru 55, 57, 58, 60, 61, 63, 64, 66 and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 as applied to claims 46, 47, 56, and 62 above, and further in view of Seo 6,323,521. Kadota does not disclose the interlayer insulating film comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide. However, Seo discloses (see, for example, FIG. 6D) a semiconductor device comprising a gate insulating interlayer (interlayer insulating film) 219 over a thin film transistor. In column 9, lines 3-8, Seo discloses the gate insulating interlayer as being silicon

oxide or other suitable material. The gate insulating interlayer covers the gate electrode and active region of the thin film transistor, and provides an adequate material for making contact holes. The contact holes are used to form contacts to source and drain regions of a thin film transistor. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide for the interlayer insulating film in order to cover the gate electrode and active region of the thin film transistor and provides an adequate material for making contact holes, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim 52-55, Kadota discloses (see, for example, FIG. 1) a semiconductor device comprising a thin film transistor formed over a TFT substrate (insulating surface) 0 wherein the thin film transistor comprises a semiconductor film 2, source and drain region S/D, channel forming region, gate insulating film, gate electrode 3; first inter-layer insulating film (first interlayer insulating film) 4, electrodes (conductive layer) 7, second inter-layer insulating film (passivation film) 5, color filter 9R/9G/9B, and pixel electrode 1. Kadota does not disclose the second inter-layer insulating film (passivation film) comprising at least a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide. However, Seo discloses (see, for example, FIG. 6D) a semiconductor device comprising a passivation film (second interlayer insulating film) 231 over a thin film transistor. In column 10, lines 2-5, Seo discloses the passivation film as being silicon oxide or silicon nitride. The passivation film covers the source and drain electrodes of the thin film transistor and provides an adequate

material for making contact holes. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use a material selected from the group consisting of silicon nitride, silicon oxide and nitrated silicon oxide in order to cover the source and drain electrodes of the thin film transistor and provide an adequate material for making contact holes, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

7. Claims 71, 73 and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 as applied to claims 46, 47, 56, and 62 above, and further in view of Ha 5,677,207. Kadota does not disclose LDD regions in contact with the channel forming region. However, Ha discloses (see, for example, FIG. 3G) a semiconductor device comprising LDD regions 38 in contact with a channel area 32a. In column 1, lines 48-63, Ha discloses that LDD areas reduce the electric field between the drain and channel area. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include the LDD regions of Ha in Kadota's invention in order to reduce the electric field between the drain and channel area, and reduce leakage current.

8. Claims 72, 75, and 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Seo '521 as applied to claims 48-55, 57, 58, 60, 61, 63, 64, 66 and 67 above, and further in view of Ha 5,677,207. Kadota in view of Seo does not disclose LDD regions in contact with the channel forming region. However, Ha discloses (see, for example,

FIG. 3G) a semiconductor device comprising LDD regions 38 in contact with a channel area 32a. In column 1, lines 48-63, Ha discloses that LDD areas reduce the electric field between the drain and channel area. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include the LDD regions of Ha in Kadota in view of Seo in order to reduce the electric field between the drain and channel area, and reduce leakage current.

9. Insofar as definite, claims 77, 78, 83, and 86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 as applied to claims 46, 47, 56, and 62 above, and further in view of Matsumoto 5,323,042. Kadota does not disclose a driver circuit comprising a second thin film transistor, wherein the pixel matrix circuit and the driver circuit are over a same substrate. However, Matsumoto discloses (see, for example, FIG. 1) a semiconductor device comprising a thin film transistor 12 for a matrix circuit and thin film transistor for a peripheral driving circuit (driver circuit) 13. In column 1, lines 8-48, Matsumoto states that an active matrix type liquid crystal display comprises a matrix circuit for applying an electric field and a peripheral driving circuit for driving the matrix circuit. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include a driver circuit in order to drive the matrix circuit in Kadota's LCD device.

10. Claims 79 thru 82, 84, 85, 87 and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Seo '521 as applied to claims 48-55, 57, 58, 60, 61, 63, 64, 66 and 67 above, and further in view of Matsumoto 5,323,042. Kadota in view of Seo does not disclose a driver circuit comprising a second thin film transistor, wherein the pixel

matrix circuit and the driver circuit are over a same substrate. However, Matsumoto discloses (see, for example, FIG. 1) a semiconductor device comprising a thin film transistor 12 for a matrix circuit and thin film transistor for a peripheral driving circuit (driver circuit) 13. In column 1, lines 8-48, Matsumoto states that an active matrix type liquid crystal display comprises a matrix circuit for applying an electric field and a peripheral driving circuit for driving the matrix circuit. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include a driver circuit in order to drive the matrix circuit of Kadota in view of Seo.

11. Insofar as definite, claim 68 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 as applied to claims 46, 47, 56, and 62 above, and further in view of Mikoshiba 5,499,123. Kadota discloses a planarization film (resin film) 10. In column 5, lines 60-65, Kadota discloses the planarization film comprising an acrylic resin or polyimide resin used as an organic transparent material. Kadota does not disclose an electrode over the organic resin film; and an oxide film of the first electrode in direct contact with at least a portion of a surface of the first electrode, wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and wherein a storage capacitor comprises the first and the second electrode with oxide film interposed therebetween. However, Mikoshiba discloses (see, for example, FIG. 3B) a semiconductor device comprising a capacitance element 400 wherein the capacitance element comprises a shading layer (electrode) 312, insulating layer (oxide film) 314, and transparent layer (second electrode) 308. In column 4, lines 57-64, Mikoshiba discloses that a bias voltages can be applied to the capacitance element so that a brighter, clearer image can be

attained. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include an electrode over the organic resin film; and an oxide film of the first electrode in direct contact with at least a portion of a surface of the first electrode, wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and wherein a storage capacitor comprises the electrode and the pixel electrode with oxide film interposed therebetween in order to apply a bias voltage to an LCD device so that a brighter, clearer image may be attained.

12. Claims 69 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota et al. '550 in view of Seo '521 as applied to claims 48-55, 57, 58, 60, 61, 63, 64, 66 and 67 above, and further in view of Mikoshiba 5,499,123. Kadota in view of Seo discloses a planarization film (resin film) 10. In column 5, lines 60-65, Kadota discloses the planarization film comprising an acrylic resin or polyimide resin used as an organic transparent material. Kadota in view of Seo does not disclose an electrode over the organic resin film; and an oxide film of the first electrode in direct contact with at least a portion of a surface of the first electrode, wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and wherein a storage capacitor comprises the first electrode and the pixel electrode with the oxide film interposed therebetween. However, Mikoshiba discloses (see, for example, FIG. 3B) a semiconductor device comprising a capacitance element 400 wherein the capacitance element comprises a shading layer (first electrode) 312, insulating layer (oxide film) 314, and transparent layer (second electrode) 308. In column 4, lines 57-64, Mikoshiba discloses that a bias voltage can be applied to the capacitance element so that a brighter, clearer image can be attained.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include the first electrode over the organic resin film; and an oxide film of the first electrode in direct contact with at least a portion of a surface of the first electrode, wherein the pixel electrode is in direct contact with at least a portion of the oxide film, and wherein a storage capacitor comprises the first and the second electrode with oxide film interposed therebetween in order to apply a bias voltage to an LCD device so that a brighter, clearer image may be attained.

Response to Arguments

13. Applicant's arguments with respect to claims 46-88 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 703-305-5695. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached at 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Eugene Lee
November 22, 2003

GEORGE ECKERT
PRIMARY EXAMINER